REMARKS

Claims 1-24 are pending in the application.

Claims 1-24 are rejected.

I. 35 U.S.C. § 102

The Office Action rejected claims 1-24 under 35 U.S.C. 102(e) as being anticipated by Beletsky (U.S. Patent No. 6,681,377). This rejection is respectfully traversed for the reasons set forth below.

The present invention relates to determining a clock gating function for a set of clocked state-holding elements. More specifically, the present invention relates to determining this function through the steps of (i) determining which of the data inputs are common for the elements in the set; and then determining, for each element in the set, the conditions under which that element will hold its current value based only on the common inputs; and (ii) combining for each element the determined conditions to form the clock gating function for that element.

Beletsky, by contrast, is concerned with preventing "hold time violations." Beletsky states that such violations occur when the "transmitting device [the data input cone] removes a data signal before a receiving device [the clocked state holding element] had properly saved it." See, col. 2., lines 9-12. For a circuit having one or more primary input clocks, Beletsky describes a method in which a "bit field" is created for each net in a clock cone. This "bit field" shows whether a positive edge or negative edge of the primary input clock may change the net. A similar "bit field" for the nets in the data input cones is created. The two "bit fields" produced are then ANDed together, the result showing nets which are susceptible to hold time violations. "Predicting logic" is then built for these nets. Accordingly, there are a number of significant differences between the present invention as limited by claim 1 and Beletsky.

Turn now to claim 1. Claim 1 recites "a method of determining a clock gating function," and specific steps to provide this determination. A clock gating function is the relationship between a number of inputs and the decision as to whether the clock signal is to be gated. This function can be fabricated as gating circuitry. Beletsky, by contrast, takes an existing clock gating circuit and analyzes it for potential hold time violations. Therefore, Beletsky does not "determine a clock gating function." and does not modify a clock gating function. The analysis described in Beletsky produces a result based on the clock gating circuitry (the embodiment of the clock gating function). If Beletsky's methodology were to change this function, the circuit would be changed, and the analysis would be useless. Beletsky only teaches the notion of analyzing an existing circuit to determine potential hold time violations, and then adding supplementary circuitry to avoid potential hold time violations. There is no determination of a clock gating function.

Specifically, in Beletsky's illustrative circuit, the clock cone creating 'G', specifically the flip flop 1025 and AND gate 1030 in Figure 7, is modified to form the circuit of Figure 11. This circuit maintains the components referenced as "1025" and "1030" (hence presents the same "clock gating function"), with additional circuitry to protect against hold time violations.

Claim 1 also recites "determining, for each element, the conditions under which the element will hold its current value based only on the common inputs." The method of Beletsky describes creating a bit field containing "information as to whether the positive edge [clock] input may change the net or whether a negative edge [clock] input may change the net." Beletsky teaches a system entirely different to the present application, since in Beletsky the method searches for change (i.e. it looks for potential problems which occur when a flip-flop is

to be switched), in the present application the method searches for "no change", i.e., it looks for potential savings when the flip-flop is not to be switched.

There is also no mention of Beletsky of seeking "common inputs." Each and every clock cone is analyzed. Consequently there is no teaching of a method specifically seeking "common inputs."

Finally, the present application describes "combining, for each element, the determined conditions to form the clock gating function for that element." As mentioned above, Beletsky fails to create a clock gating function. Beletsky takes an existing gating circuit, analyzes it for potential hold time violations, and adds supplementary circuitry to avoid such problems. There is no teaching of using the analysis performed as part of the method of Beletsky to form a clock gating function.

Accordingly it is submitted that Beletsky fails to teach the invention as recited in claim 1. Independent claims 19, 20 and 24 are substantially similar to claim 1 and, accordingly, the same arguments made with respect to the patentability of claim 1 are applicable.

Dependent claims 2-18 and 21-23 depend directly or indirectly from claims 1 and 20, respectively, and are also patentable for the reasons stated for claims 1 and 20.

II. Summary

Having fully addressed the Examiner's objections and rejections, it is believed that in view of the preceding remarks, this entire application stands in a condition for allowance. If, however, the Examiner is of the opinion that such action cannot be taken, he is invited to contact the applicants' attorney at the number and address below in order that any outstanding issues may be resolved without the necessity of issuing a further Action. An early and favorable response is earnestly solicited.

Please address all future correspondence to Intellectual Property Docket Administrator, Gibbons, Del Deo, Dolan, Griffinger & Vecchione, One Riverfront Plaza, Newark, NJ 07102-5496. Telephone calls should be made to David R. Padnes by dialing Area Code (973) 596-4671.

III. Fees

If any additional fees are due in respect to this amendment, please also charge them to Deposit Account No. 03-3839.

Respectfully submitted,

Date: 8/3/06

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